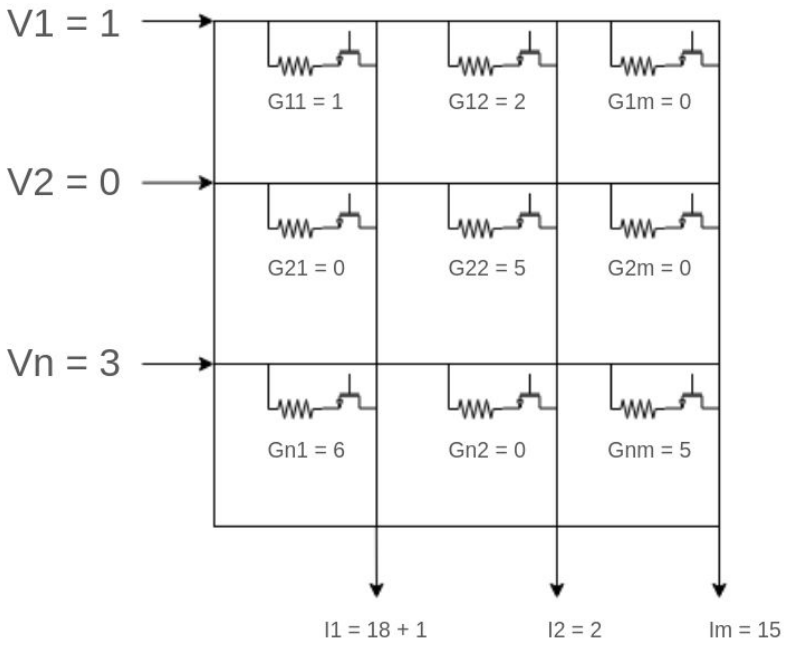
Project Plan

Sddec24-13

Project Overview

ReRam Crossbar ASIC Fabrication

- Utilize memristors to develop a crossbar matrix capable of vector matrix multiplication to perform computation
- Submit a qualifying project to Efabless using the Caravel “harness” SoC
- Revise and expand upon previous teams documentation
    - Documentation is styled in a lab walkthrough format because of the plans for co-curricular uses later



Project management style

We use the AGILE methodology.

- We use the AGILE method in short one week sprints to keep a tab on our progress
- Chosen because of the iterative nature of the methodology meshes well with the project objectives and design process
- The AGILE methodology also allows us to make sure that we are completing our objectives

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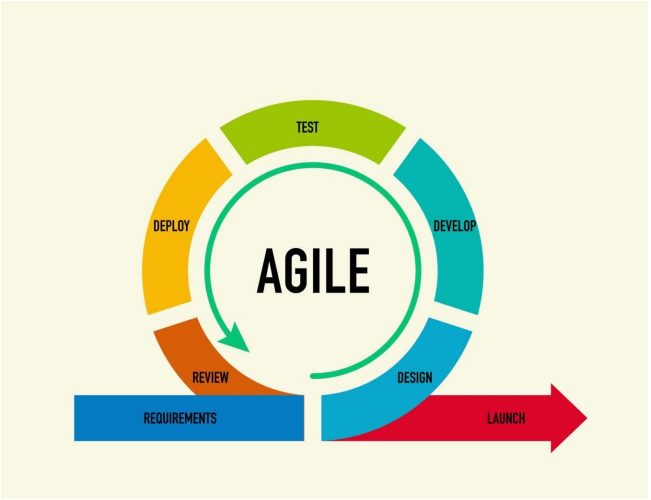
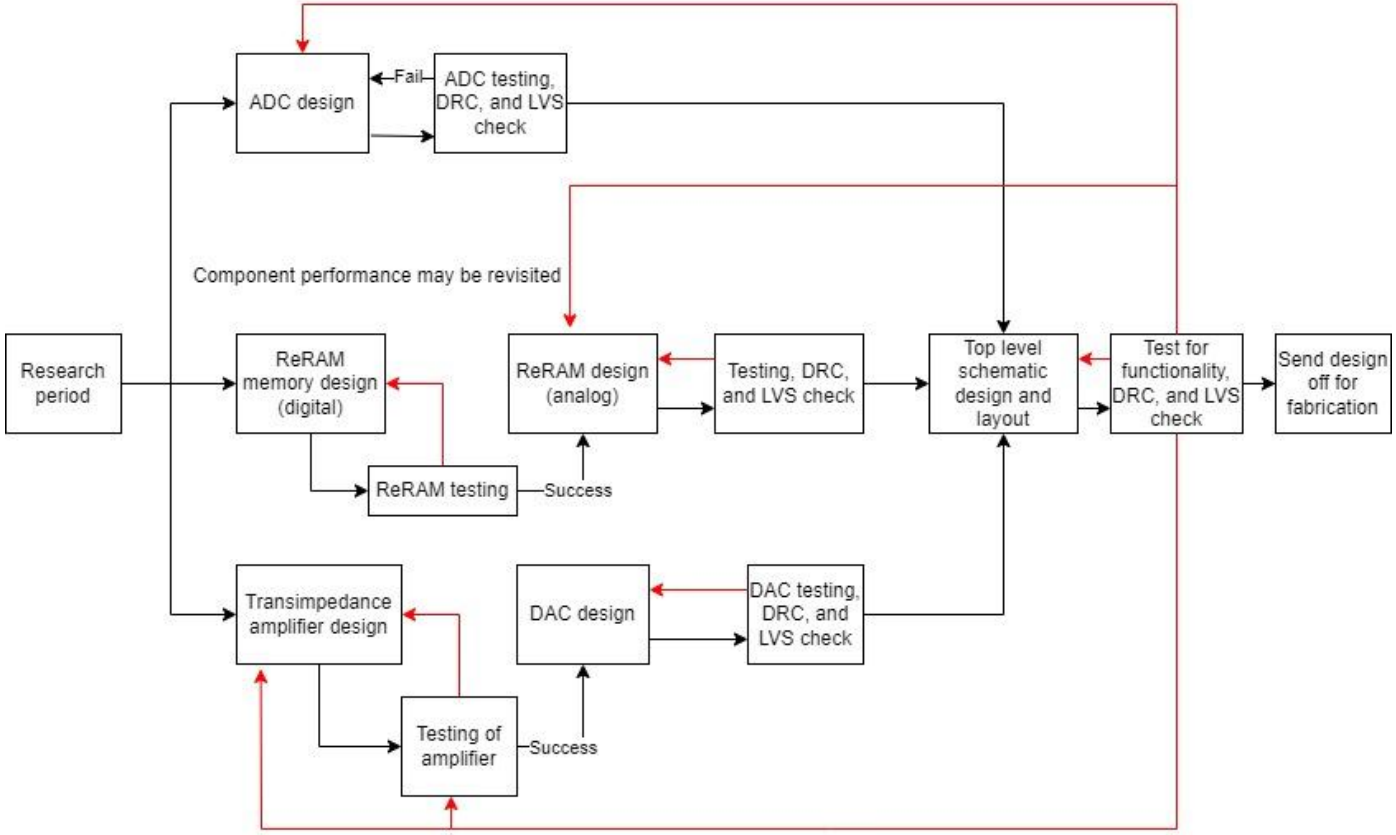


Task decomposition(high lvl)



Key milestones metrics and evaluation criteria

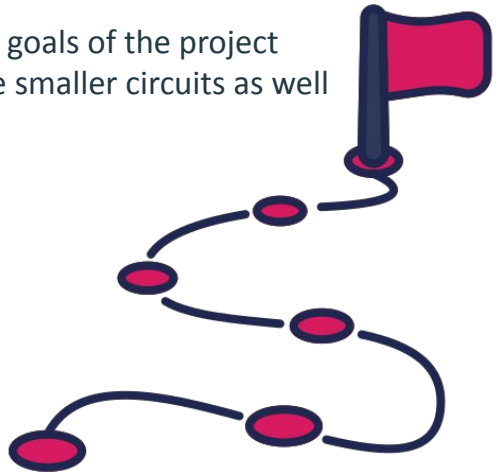
Key Milestones:

- ADC design
  - 3-4 bit resolution
- Transimpedance amplifier design
- ReRam behavioral model
- User interface design
- Full set of documentation
  - Bring up plans
  - Design documents

Evaluation Criteria:

- Compute speed and accuracy
- Energy efficiency
- Power consumption

These criteria are the overarching goals of the project and can be applied to many of the smaller circuits as well



Key risks and risk mitigation strategies

Potential Risks

- Risk of not completing the project in time for efabless submission
  - This risk can be mitigated by getting everything completed in a timely manner
- Risk of undesired general design functionality
  - This risk can be mitigated by performing and passing relative simulations and unit tests
- Risk of the final circuit not meeting client specifications
  - This risk can be mitigated by communicating clearly with the client throughout the project